Stacked PMOS is bad compared to stacked NMOS, and it's because of the PMOS having worse mobility, right? Since the mobility ratio is about 1:2, you have to scale the PMOS W/L in a 2:1 ratio just to match the NMOS performance. When you stack them, the resistance effectively doubles, so you have to compensate even more. This means for a 2-stack PMOS, the W/L ratio has to be more like 4:1, which is why it's so much worse in terms of area and speed.  
  
  
Flatten command is used to make a flat netlist.  
No hierarchies of sub\_modules is seen in flatten ed netlist  
  
Module level synthesis is preferred when we have multiple instances of same module, so that we can jyst synthesise the module once and paste the netlist, instead of synthesising same module multiple times OR for divide and conquer approach-> for a large circuit, device might not give proper connections, so just synthesise one module at a time.  
  
  
While synthesising Dff, after read\_verilog is done, we have to put in dfflibmap -liberty ../lib/sky130\_fd\_sc\_hd\_\_tt\_025C\_1v80.lib  
coz many times in flow they keep different flop library and std. cell library, so we need to tell the tool where to pick the DFF from. ( here we have all in same so we’re pointing to the same library)